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Toward Self-Assembled Ferroelectric Random Access Memories: Hard-Wired Switching Capacitor Arrays with Almost Tb/in.^{2} Densities

Paul R. Evans,[†] XinHau Zhu,[†] Paul Baxter,[†] Mark McMillen,[†] John McPhillips,[†] Finlay D. Morrison,[‡,§] James F. Scott,[‡] Robert J. Pollard,[†] Robert M. Bowman,[†] and J. Marty Gregg*,[†]

Centre for Nanostructured Media, School of Maths and Physics, Queen's University Belfast, Belfast BT7 1NN, United Kingdom, and Department of Earth Sciences, University of Cambridge, Cambridge CB2 3EQ, United Kingdom

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ABSTRACT

We report on the successful fabrication of arrays of switchable nanocapacitors made by harnessing the self-assembly of materials. The structures are composed of arrays of 20–40 nm diameter Pt nanowires, spaced 50–100 nm apart, electrodeposited through nanoporous alumina onto a thin film lower electrode on a silicon wafer. A thin film ferroelectric (both barium titanate (BTO) and lead zirconium titanate (PZT)) has been deposited on top of the nanowire array, followed by the deposition of thin film upper electrodes. The PZT nanocapacitors exhibit hysteresis loops with substantial remnant polarizations, while although the switching performance was inferior, the low-field characteristics of the BTO nanocapacitors show dielectric behavior comparable to conventional thin film heterostructures. While registration is not sufficient for commercial RAM production, this is nevertheless an embryonic form of the highest density hard-wired FRAM capacitor array reported to date and compares favorably with atomic force microscopy read–write densities.

The importance of data storage to the smooth operation of the modern world has meant that a great deal of research into different memory technologies has been an ongoing high-profile theme in both industry and academic research laboratories.[1] One of the many driving factors influencing this research has been the quest to replace dynamic random access memory (DRAM), and to some extent the combination of DRAM and hard drives, with nonvolatile random access memory (NVRAM). Use of NVRAM as the so-called "universal memory"[2] would both obviate the need to continuously refresh data held in DRAM and avoid the rather awkward interplay between the DRAM chips and ferromagnetic hard drives.

While there are many candidates for future NVRAM, those involving permanent charge storage in capacitor structures, using ferroelectric materials, perhaps represent the most natural progression from DRAM, and indeed, low-density forms of ferroelectric RAM (FRAM) are already in commercial use.[3,4] There is also interest in ferroelectric-based media as a variation on magnetic hard disk technology.[5]

As with all forms of electronic devices, miniaturization and reductions in production cost are constant driving forces in memory development. Unfortunately though, standard "top-down" photolithographic processing becomes progressively more expensive and more difficult to implement as feature sizes of electronic elements decrease into the realms of tens of nanometers. The lithography associated with top-down fabrication can also significantly compromise functional properties; damage due to aggressive etching environments, particularly at feature edges and peripheral chip areas, can cause significant variations in, for example, switching behavior of ferroelectric capacitors.[6,7] When coupled with the need for more sensitivity to the amount of switched charge in nanometer feature size FRAMs, edge damage can have dramatic ramifications for reliability. Nanoscale miniaturization therefore comes at a price unless the thermodynamics and kinetics of material behavior can be used to create nanoscale electronic devices without any top-down patterning. Attempting to do exactly this, through "self-assembly", has been an area of intense recent research.[8] Within the field of nanoscale ferroelectric capacitors alone,

* Corresponding author. E-mail: m.gregg@qub.ac.uk.
[†] Queen's University Belfast.
[‡] University of Cambridge.
[§] Current address: School of Chemistry, University of St. Andrews, St. Andrews, Fife, KY16 9ST, United Kingdom.

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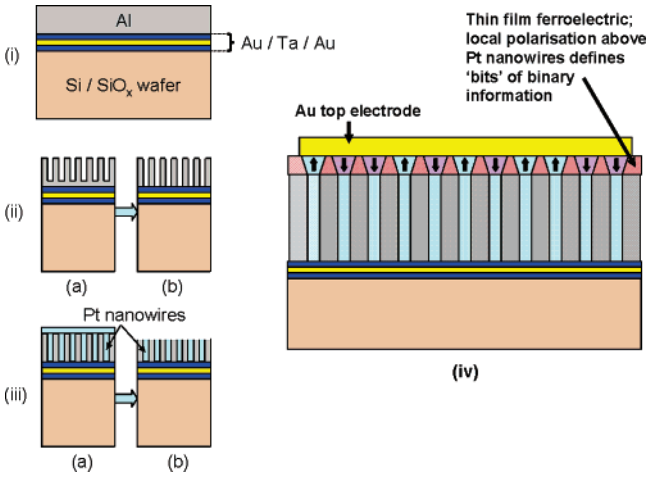

Figure 1. Schematic cross-sections of the processing steps associated with the creation of the self-assembled nanocapacitor array: (i) deposition of thin film multilayer electrode and aluminum; (ii) electrolytic anodization of aluminum to form nanopores (a), and NaOH etch (b); (iii) electrolytic deposition of Pt nanowires to the point of overgrowth onto the alumina surface (a), followed by low-angle blanket ion etch (b); (iv) ferroelectric film and top electrode deposition.

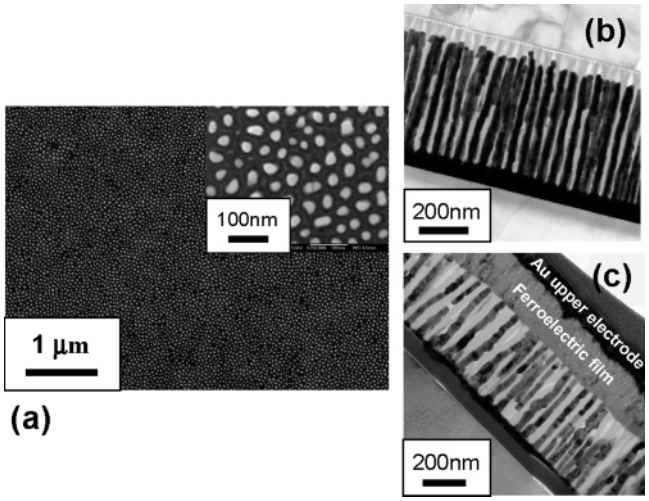

Figure 2. Electron microscopy images illustrating the creation of the Pt nanowire arrays (plan-view scanning electron microscopy image (a) and cross-sectional transmission electron microscope (TEM) image (b)); cross-sectional overview (TEM) of the completed nanocapacitor array.

several groups have already shown the potential for self-assembly in creating extremely high storage densities.[9−15] However, progress is in its early stages, and working nanoscale "self-assembled" devices are still a long way from becoming a reality.

It is in this context that we report results from a research program in which thin film arrays of nanoscale capacitor structures, hard-wired using Pt nanowires, have been made through self-assembly. The dimensions of the individual capacitor structures, and their lateral spacing, mean that the nominal bit density is of the order of $10^{11}-10^{12}$ bits per square inch; this sets a new paradigm in hard-wired solid-state memory, and even though similar densities have been demonstrated using scanning probe arrangements,[16−20] the advantage of this self-assembled structure is that potentially no moving parts are needed.

A schematic diagram of the processing steps involved in creating the final structure is shown in Figure 1. Initially (Figure 1i), a multilayered tantalum−gold thin film bottom electrode and a thin film (∼450 nm) of aluminum were sputter-coated onto a SiO_x-silicon wafer.[21] The complex multilayered lower electrode was a necessary development to keep reasonable conductivity (through the Au layer) but also have sufficiently strong adhesion between the lower electrode and the substrate so that delamination did not occur during electrolytic anodization of the aluminum. We then placed the coated wafer into a bath of cooled (2 °C) weak sulfuric acid (0.3 M), connecting it up as the anode in an electrolytic circuit using Pt as the cathode. Application of a voltage (20 V) induced the oxidation of the aluminum and the associated formation of nanopores (Figure 1iia).[22] Any alumina at the bottom of the nanopores was removed by a subsequent chemical etch (0.1 M NaOH), locally exposing the lower electrode (Figure 1iib). Then we placed the wafer into another electrolytic cell containing a 0.2 M chloroplatinic acid salt solution and applied a voltage using a potentiostat. A typical deposition voltage was −0.1 V with respect to a saturated calomel electrode. Because the only conducting regions of electrode exposed to the solution were those at the bottom of the nanopores, electrolytic Pt deposition could only occur within the pores, forming nanowire arrays. The deposition current was monitored during the deposition, and a sudden increase was seen when the wires reached the top of the pores. The deposition was then allowed to continue until the current was no longer increasing, indicating that overgrown wires had merged to form a continuous film on the surface (Figure 1iiia). The sample was then blanket argon ion etched at a low angle to remove this film, leaving the top of the nanowires level with the top of the alumina (Figure 1iiib). Ferroelectric layers were deposited either using pulsed laser deposition (for the barium titanate (BTO); for typical fabrication information, see ref 23) or "misted" chemical solution deposition (for lead zirconium titanate (PZT); for typical fabrication information, see ref 24). Sputtering of gold or platinum upper electrodes completed the structure (Figure 1iv). Figure 2 presents micrographs illustrating the formation of the Pt nanowire array, where clear separation between individual nanowires is evident (plan view image, Figure 2a), as is their relatively straight morphology (cross section image, Figure 2b); Figure 2c shows a cross section of the completed test device. It is noteable that the relatively high processing temperature needed for the oxide ferroelectric layer (∼600 °C) causes some degradation to the nanowire morphology. Indeed, in early work where gold nanowires were used, the annealing required for ferroelectric processing caused complete detachment of the nanowires from the Au/Ta/Au lower electrode. Even with Pt nanowires, if ferroelectric processing temperatures are too high (>∼650 °C), large areas of detachment occur, as have been noted in cross-sectional TEM and in mapping using surface piezoforce microscopy, where large regions of film could not be poled. Work is ongoing

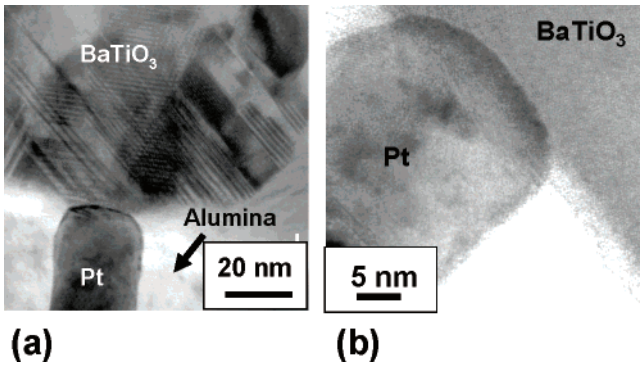

Figure 3. Relatively high magnification images (cross-sectional TEM) showing the successful contact between the Pt nanowires and ferroelectric films.

using small amounts of oxygen in the initial aluminum thin film to improve the thermal stability of the pore structures.

The active material for data storage is the ferroelectric thin film, with its state of polarization (either "up" or "down") defining the binary "1" and "0" of the memory. The polarization direction is switched by applying an electric field between the Pt nanowire and the common top electrode. The dimensions of each bit are defined by the field emanating from the tip of each Pt nanowire. The limit for planar bit size is currently driven by the need for the quantity of switched charge to be large enough to be sensed over the parasitic capacitance of the bit-line of the surrounding architecture. For our 20 nm diameter Pt wires, assuming a switchable polarization of $\sim$50 μC/cm^2 for the ferroelectric, we can estimate the switched charge per bit of only ca. 1.6 $\times$ 10^{-16} C. This corresponds to $\sim$1000 electrons and is at the present limit for electrical sensing.[25] The nanowires are laterally electrically insulated from each other by alumina and could thus be used as discrete electrodes. In the current structure, the Pt nanowires are not yet individually addressable through the lower electrode, but this is, along with the creation of perfect registry of nanowires, an important area for future development. Our structure does, however, represent a "proof of concept" that nanoscale memory arrays could be constructed without "top-down" patterning.

Figure 3 shows transmission electron microscopy (TEM) images of a cross-section of the contact between the Pt nanowires and the ferroelectric layer, critical in making the device operational. Figure 4 illustrates the functional characteristics of the arrays: in the BTO systems, the almost frequency independent behavior of the low-field permittivity, and relatively low dielectric loss, imply that electrically sound capacitor structures have been made. The BTO films were not, however, able to withstand the fields necessary for ferroelectric switching and complete saturation. This contrasts with the PZT-based nanocapacitor arrays, which although being somewhat more lossy, showed genuine switching with remnant polarizations, taken using both Sawyer−Tower (Figure 4a, see ref 26) and the "PUND" measurement techniques (Figure 4b, see ref 27), comparable to bulk ($\sim$50 μC cm^{-2}, see Figure 4b). The slightly high coercive field of ca. 500 kV/cm is not yet understood, but planar features, possibly extremely fine domains, such as those seen clearly

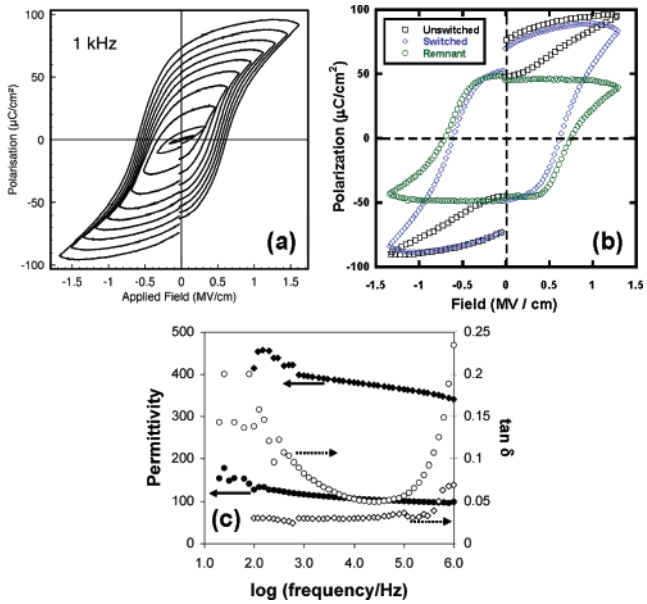

Figure 4. Room-temperature polarization-field hysteresis loops (at 1 kHz) from nanocapacitor arrays with PZT as the ferroelectric layer using a Sawyer−Tower circuit (a),[26] and "PUND" measurement technique (b)[27] with triangular pulse waveforms. Note the remnant polarization of $\sim$50 μC cm^{-2} obtained through "PUND"; (c) frequency dependence of the low-field relative permittivity and dielectric loss tangent at room temperature for a nanocapacitor array using $BaTiO_3$ (diamonds) and $PbZr_{0.4}Ti_{0.6}O_3$ (circles) as the ferroelectric layer.

in $BaTiO_3$ (Figure 3a), are frequently observed and may be partly responsible for the disruption of switching.

While the potential for development of this self-assembled nanocapacitor array is exciting, there are several issues needing more work:

(1) We recognize that the ferroelectric "bits" may require registry and wiring in order to achieve individual addressability. In this work, we sought to investigate and demonstrate the viability of thin film AAO templates, integrated into thin film heterostructures, for creating high-density operational bit storage. Having done this, attention turns to the engineering challenge of registry and electrode addressability. Work is presently underway in this regard using recognized approaches such as imprint lithography on the aluminum film pre-anodization;[28]

(2) The growth of the ferroelectric needs to be optimized to reduce the coercive fields;

(3) The thickness of the ferroelectric needs to be significantly reduced so that the polarized regions above each Pt nanowire do not overlap as a result of lateral field-spreading through the ferroelectric film. This needs to be achieved without compromising functional properties.

This third issue has been addressed to some extent. Functional data presented in Figure 4 was for ferroelectric films >100 nm in thickness. Modeling of the potential distribution associated with the nanowire array has been performed using frameworks originally devised for scanning probe microscopy research.[29−31] This shows that, for the films of the order of 100 nm and greater, the system largely behaves as though the nanowires were a continuous lower

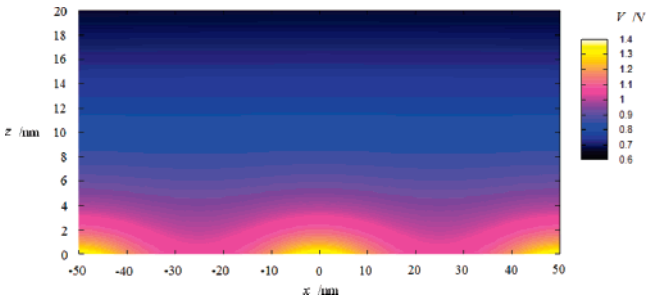

Figure 5. Modeled potential distribution above the Pt nanowires in *c*-axis oriented $BaTiO_3$ (*c*-axis perpendicular to the ferroelectric film surface), using approaches used previously for describing potential associated with scanning probe microscopy tips.[29−31] Even at ∼20 nm, the potential distribution resembles that of a parallel-plate geometry.

electrode, and this conventional geometry was assumed in calculations of both the polarization and permittivity values presented. Furthermore, modeling suggests that, for individual bits to be spatially resolved, the ferroelectric thickness should be considerably thinner, indicated by the potential distribution map shown in Figure 5 for a 20 nm ferroelectric film. Work is currently underway to make films in this ultrathin regime.

In summary, a novel structure has been made in which ferroelectric films have been deposited onto arrays of self-assembled platinum nanowires, laterally electrically isolated from each other by aluminum oxide. The nanowire−ferroelectric interface has been shown to be of sufficient quality that ferroelectric switching can be induced by dropping potential between the nanowire and a common macroscopic upper electrode. The scale of the nanowire array is such that bit densities approach the Tb in.$^{-2}$.

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